CLAIMS:

1. A method for designing an integrated circuit, the method comprising:

determining logic requirements for an intended set of applications for the integrated circuit;

determining at least one common logic function for the intended set of applications for the integrated circuit;

identifying an approximate number of configurable logic blocks and at least one fixed logic circuit that, when combined to operate cooperatively, meet a substantial portion of the logic requirements for the intended set of applications for the integrated circuit;

designing the integrated circuit to include the approximate number of configurable logic blocks formed as a fabric and arranged to surround an opening in the fabric;

designing the integrated circuit to include the at least one fixed logic circuit in the opening in the fabric; and

designing the integrated circuit to include interconnecting logic that interfaces the at least one fixed logic circuit to the fabric.

2. The method of claim 1, further comprising:

selecting a die size for the integrated circuit; and

designing the integrated circuit such that the configurable logic blocks and the at least one fixed logic circuit fit within a targeted die size.

3. The method of claim 1, further comprising:

selecting a process for manufacturing of the integrated circuit, wherein the process involves a minimum dimension size for the integrated circuit; and

selecting a die size for the integrated circuit considering the process, the approximate number of configurable logic blocks and the at least one fixed logic circuit.

4. The method of claim 1, wherein the at least one fixed logic circuit is selected from the group consisting of digital signal processors, microprocessors, physical layer interfaces, link layer interfaces, network layer interfaces, audio processors, video graphics processors, and applications specific integrated circuits.

5. The method of claim 1, wherein the intended applications include at least one of communications applications, system-on-a-chip applications, image processing applications, parallel procesing applications, networking applications, serial processing applications, and prototyping applications.

6. The method of claim 1, wherein the logic requirements are characterized by parameters including at least one of data processing requirements, data storage requirements, data throughput requirements, instruction set type, and instruction set contents.

7. The method of claim 1, wherein:

the integrated circuit occupies a die area; and

the fixed logic circuit occupies less than a predetermined percentage of the die area.

8. A method for designing an integrated circuit, the method comprising:

identifying an intended set of applications for the integrated circuit;

determining logic requirements for the intended set of applications for the integrated circuit;

determining at least one common logic function for the intended set of applications for the integrated circuit;

identifying an approximate number of configurable logic blocks that meets the programmable logic requirements of a substantial portion of the intended set of applications;

selecting a fixed logic circuit that is operable to meet the at least one common logic function for the intended set of applications for the integrated circuit;

designing the integrated circuit to include the fixed logic circuit and a fabric formed of the approximate number of configurable logic blocks, wherein the fixed logic circuit and the fabric operate cooperatively to substantially meet the logic requirements of the intended set of applications for the integrated circuit; and

designing the integrated circuit to include interconnecting logic that interfaces that interfaces the fixed logic circuit to the fabric.

9. The method of claim 8, further comprising:

selecting a die size for the integrated circuit; and

designing the integrated circuit such that the configurable logic blocks and the fixed logic circuit fit within a targeted die size.

10. The method of claim 8, further comprising:

selecting a process for manufacturing of the integrated circuit, wherein the process involves a minimum dimension size for the integrated circuit; and

selecting a die size for the integrated circuit considering the process, the approximate number of configurable logic blocks and the fixed logic circuit.

11. The method of claim 8, wherein the fixed logic circuit is selected from the group consisting of digital signal processors, microprocessors, physical layer interfaces, link layer interfaces, network layer interfaces, audio processors, video graphics processors, and applications specific integrated circuits.

12. The method of claim 8, wherein the intended applications include at least one of communications applications, system-on-a-chip applications, image processing applications, parallel procesing applications, networking applications, serial processing applications, and prototyping applications.

13. The method of claim 8, wherein the logic requirements are characterized by parameters including at least one of data processing requirements, data storage requirements, data throughput requirements, instruction set type, and instruction set contents.

14. The method of claim 8, wherein:

the integrated circuit occupies a die area; and

the fixed logic circuit occupies less than a predetermined percentage of the die area.

15. A method for designing an integrated circuit, the method comprising:

identifying an intended set of applications for the integrated circuit;

for each of the intended set of applications, identifying logic requirements;

for each of the intended set of applications, identifying input/output requirements;

identifying an approximate number of configurable logic blocks and at least one fixed logic input/output circuit that, when combined to operate cooperatively, meet a substantial portion of the logic requirements and the input/output requirements of the intended set of applications;

designing the integrated circuit with the approximate number of configurable logic blocks arranged and interconnected to form a fabric that at least partially surrounds an opening;

designing the integrated circuit to include the at least one fixed logic input/output circuit in the opening in the fabric; and

designing the integrated circuit to include interconnecting logic that interfaces the at least one fixed logic input/output circuit to the fabric.

16. The method of claim 15, further comprising:

selecting a die size for the integrated circuit; and

designing the integrated circuit such that the configurable logic blocks and the at least one fixed logic input/output circuit fit within a targeted die size.

17. The method of claim 15, further comprising:

selecting a process for manufacturing of the integrated circuit, wherein the process involves a minimum dimension size for the integrated circuit; and

selecting a die size for the integrated circuit considering the process, the approximate number of configurable logic blocks and the at least one fixed logic input/output circuit.

18. The method of claim 15, wherein the at least one fixed logic input/output circuit is selected from the group consisting of high speed serial input/output circuits and high speed parallel input/output circuits.

19. The method of claim 15, wherein the intended applications include at least one of communications applications, system-on-a-chip applications, image processing applications, parallel procesing applications, networking applications, and prototyping applications.

20. The method of claim 15, wherein the input/output requirements are characterized by parameters including at least one of bit rate input, bit rate output, data width, address width, parallel bus frequency.

21. The method of claim 15, wherein:

the integrated circuit occupies a die area; and

the at least one fixed logic input/output circuit occupies less than a predetermined percentage of the die area.

22. The method of claim 15, wherein the at least one fixed logic input/output circuit resides at an edge of the fabric.

23. A method for designing an integrated circuit, the method comprising:

identifying an intended set of applications for the integrated circuit;

determining logic requirements for the intended set of applications for the integrated circuit;

determining at least one common logic function for the intended set of applications for the integrated circuit;

selecting a fixed logic circuit that is operable to meet the at least one common logic function for the intended set of applications for the integrated circuit;

identifying input/output requirements for the intended set of applications for the integrated circuit;

identifying a fixed logic input/output circuit that meets a substantial portion of the input/output requirements for the intended set of applications for the integrated circuit;

identifying an approximate number of configurable logic blocks that, in combination with the fixed logic circuit and the fixed logic input/output circuit, substantially meets the logic requirements for the intended set of applications for the integrated circuit; and

designing the integrated circuit to include the approximate number of configurable logic blocks, the fixed logic circuit, and the fixed logic input/output circuit.

24. The method of claim 23, further comprising:

selecting a die size for the integrated circuit; and

designing the integrated circuit such that the approximate number of configurable logic blocks, the fixed logic circuit, and the fixed logic input/output circuit fit within a targeted die size.

25. The method of claim 23, further comprising:

selecting a process for manufacturing of the integrated circuit, wherein the process involves a minimum dimension size for the integrated circuit; and

selecting a die size for the integrated circuit considering the process, the approximate number of configurable logic blocks, the fixed logic circuit, and the fixed logic input/output circuit.

26. The method of claim 23, wherein the fixed logic input/output circuit is selected from the group consisting of high speed serial input/output circuits and high speed parallel input/output circuits.

27. The method of claim 23, wherein the intended applications include at least one of communications applications, system-on-a-chip applications, image processing applications, parallel procesing applications, networking applications, serial processing applications, and prototyping applications.

28. The method of claim 23, wherein logic requirements are characterized by parameters including at least one of data processing requirements, data storage requirements, data throughput requirements, instruction set type, and instruction set contents.

29. The method of claim 23, wherein the input/output requirements are characterized by parameters including at least one of bit rate input, bit rate output, data width, address width, parallel bus frequency.

30. The method of claim 23, wherein:

the integrated circuit occupies a die area; and

the fixed logic input/output circuit occupies less than a predetermined percentage of the die area.

31. The method of claim 23, wherein the fixed logic input/output circuit resides at an edge of the fabric.

32. The method of claim 23, wherein the fixed logic input/output circuit and the fixed logic processing circuit access common block ram segments.